

PROGRAMMABLE ARRAY LOGIC OR MEMORY WITH P-CHANNEL  
DEVICES AND ASYMMETRICAL TUNNEL BARRIERS

Abstract of the Disclosure

5 Structures and methods for programmable array type logic and/or memory  
with p-channel devices and asymmetrical low tunnel barrier intergate insulators are  
provided. The programmable array type logic and/or memory devices include p-  
channel non-volatile memory which has a first source/drain region and a second  
10 source/drain region separated by a p-type channel region in an n-type substrate. A  
floating gate opposing the p-type channel region and is separated therefrom by a  
gate oxide. A control gate opposes the floating gate. The control gate is separated  
from the floating gate by an asymmetrical low tunnel barrier intergate insulator.  
The asymmetrical low tunnel barrier intergate insulator includes a metal oxide  
15 insulator selected from the group consisting of  $\text{Al}_2\text{O}_3$ ,  $\text{Ta}_2\text{O}_5$ ,  $\text{TiO}_2$ ,  $\text{ZrO}_2$ ,  $\text{Nb}_2\text{O}_5$ ,  
 $\text{SrBi}_2\text{Ta}_2\text{O}_3$ ,  $\text{SrTiO}_3$ ,  $\text{PbTiO}_3$ , and  $\text{PbZrO}_3$ . The floating gate includes a polysilicon  
floating gate having a metal layer formed thereon in contact with the low tunnel  
barrier intergate insulator. And, the control gate includes a polysilicon control gate  
having a metal layer, having a different work function from the metal layer formed  
20 on the floating gate, formed thereon in contact with the low tunnel barrier intergate  
insulator.

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